

# Complementary Power Transistors

## DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series

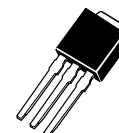
**NPN**  
**MJD31C**  
**PNP**  
**MJD32C**

Motorola Preferred Devices

**SILICON**  
**POWER TRANSISTORS**  
**3 AMPERES**  
**100 VOLTS**  
**15 WATTS**



CASE 369A–13



CASE 369–07

### MAXIMUM RATINGS

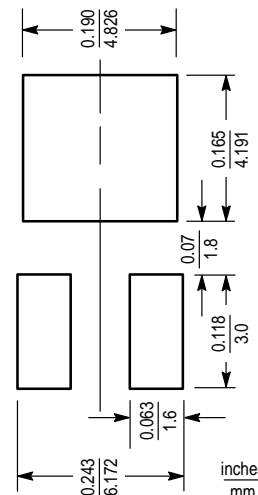
Rating	Symbol	Max	Unit
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Collector–Base Voltage	$V_{CB}$	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5	Vdc
Collector Current — Continuous	$I_C$	3	Adc
Peak		5	
Base Current	$I_B$	1	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	15	Watts
Derate above $25^\circ\text{C}$		0.12	W/ $^\circ\text{C}$
Total Power Dissipation* @ $T_A = 25^\circ\text{C}$	$P_D$	1.56	Watts
Derate above $25^\circ\text{C}$		0.012	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.3	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering Purposes	$T_L$	260	$^\circ\text{C}$

\* These ratings are applicable when surface mounted on the minimum pad size recommended.

### MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are Motorola recommended choices for future use and best overall value.

**MJD31C MJD32C****ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Collector–Emitter Sustaining Voltage (1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	—	50	$\mu\text{A}$
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB} = 0$ )	$I_{CES}$	—	20	$\mu\text{A}$
Emitter Cutoff Current ( $V_{BE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1	mA

**ON CHARACTERISTICS (1)**

DC Current Gain ( $I_C = 1\text{ A}$ , $V_{CE} = 4\text{ Vdc}$ ) ( $I_C = 3\text{ A}$ , $V_{CE} = 4\text{ Vdc}$ )	$h_{FE}$	25 10	— 50	—
Collector–Emitter Saturation Voltage ( $I_C = 3\text{ A}$ , $I_B = 375\text{ mA}$ )	$V_{CE(sat)}$	—	1.2	Vdc
Base–Emitter On Voltage ( $I_C = 3\text{ A}$ , $V_{CE} = 4\text{ Vdc}$ )	$V_{BE(on)}$	—	1.8	Vdc

**DYNAMIC CHARACTERISTICS**

Current Gain — Bandwidth Product (2) ( $I_C = 500\text{ mA}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	$f_T$	3	—	MHz
Small–Signal Current Gain ( $I_C = 0.5\text{ A}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1\text{ kHz}$ )	$h_{fe}$	20	—	—

(1) Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .(2)  $f_T = |h_{fe}| \cdot f_{test}$ .

TYPICAL CHARACTERISTICS

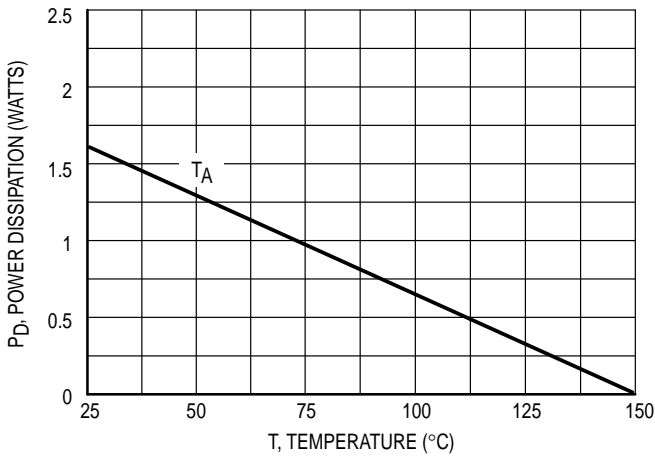
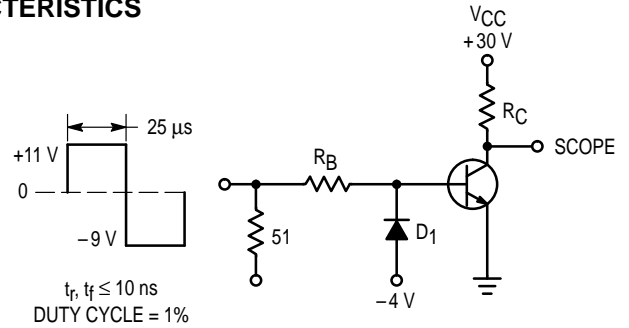


Figure 1. Power Derating



$R_B$  and  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS  
 $D_1$  MUST BE FAST RECOVERY TYPE, e.g.:  
 1N5825 USED ABOVE  $I_B \approx 100$  mA  
 MSD6100 USED BELOW  $I_B \approx 100$  mA  
 REVERSE ALL POLARITIES FOR PNP.

Figure 2. Switching Time Test Circuit

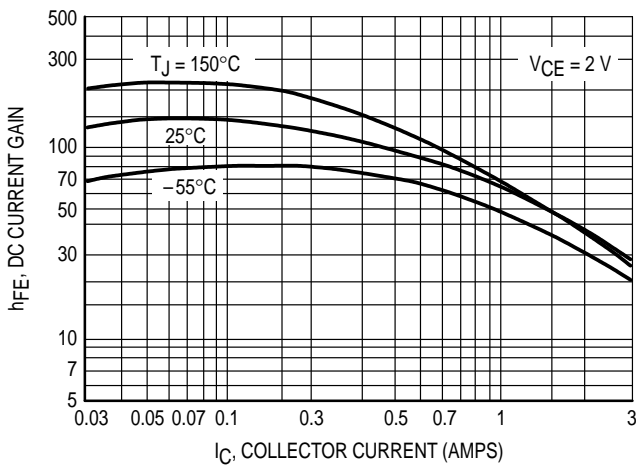


Figure 3. DC Current Gain

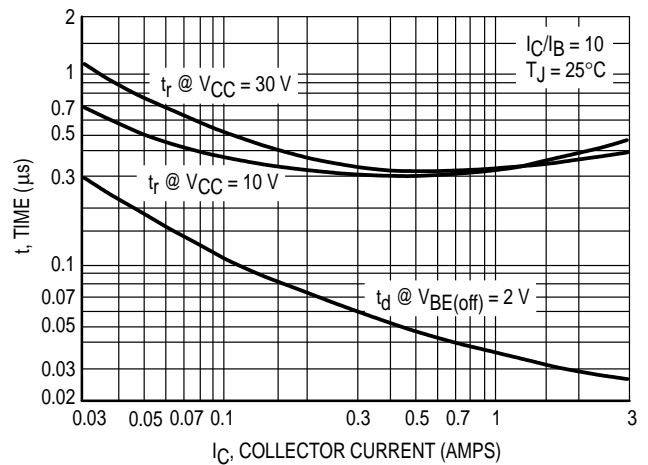


Figure 4. Turn-On Time

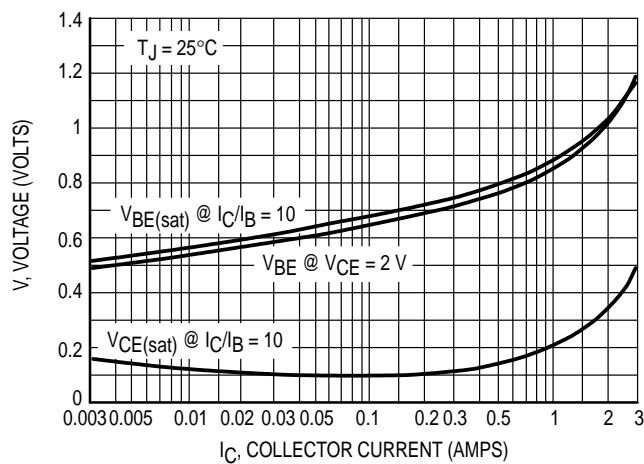


Figure 5. "On" Voltages

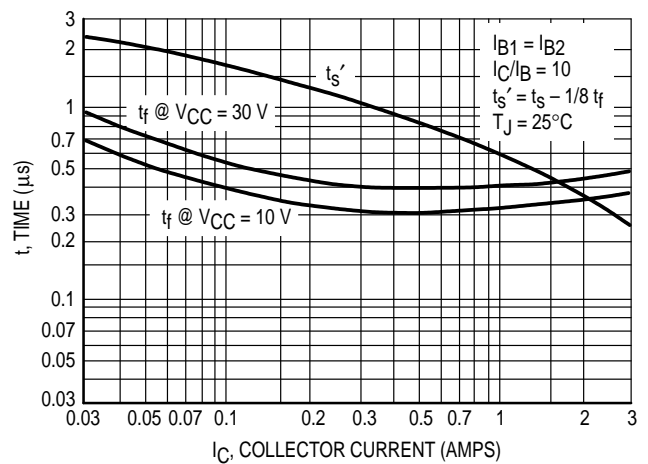
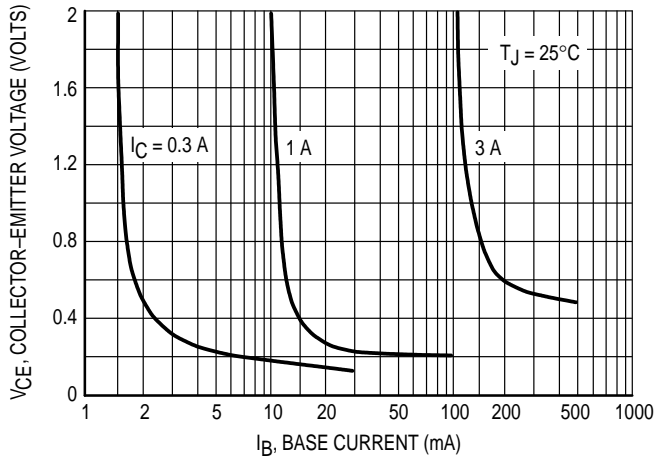
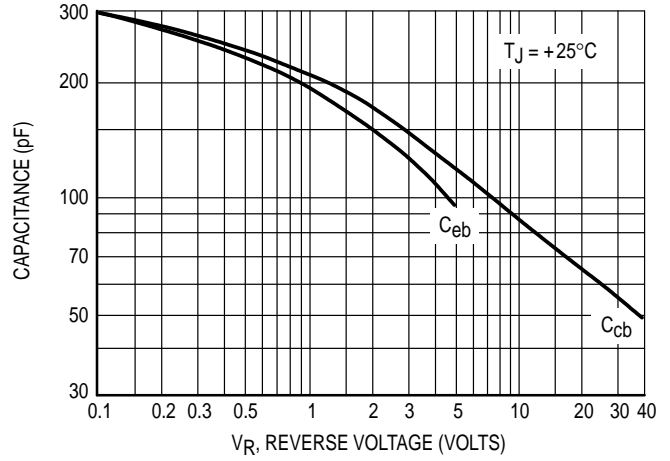


Figure 6. Turn-Off Time

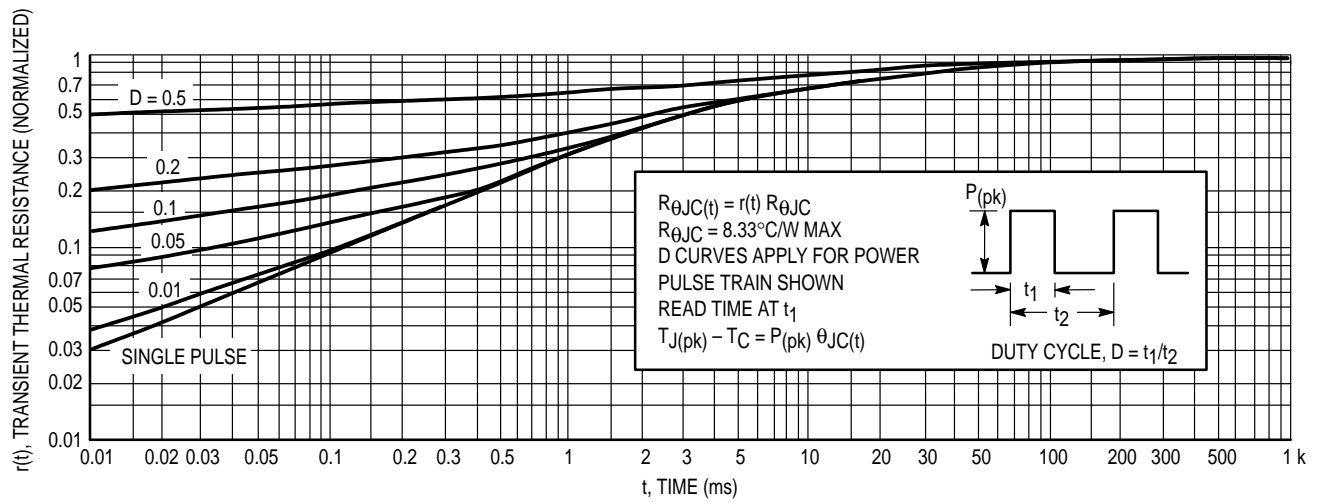
**MJD31C MJD32C**



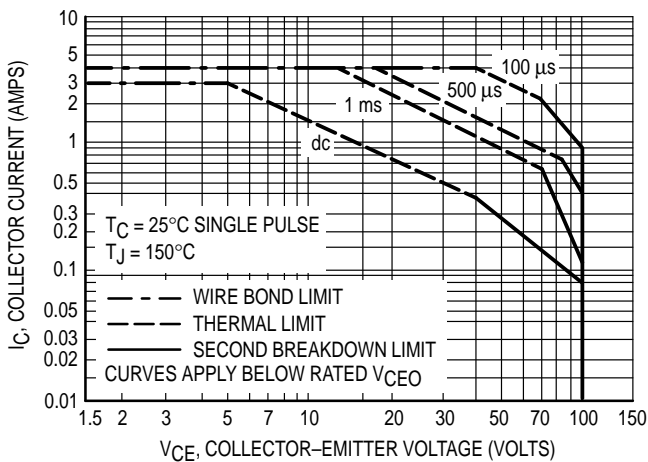
**Figure 7. Collector Saturation Region**



**Figure 8. Capacitance**



**Figure 9. Thermal Response**

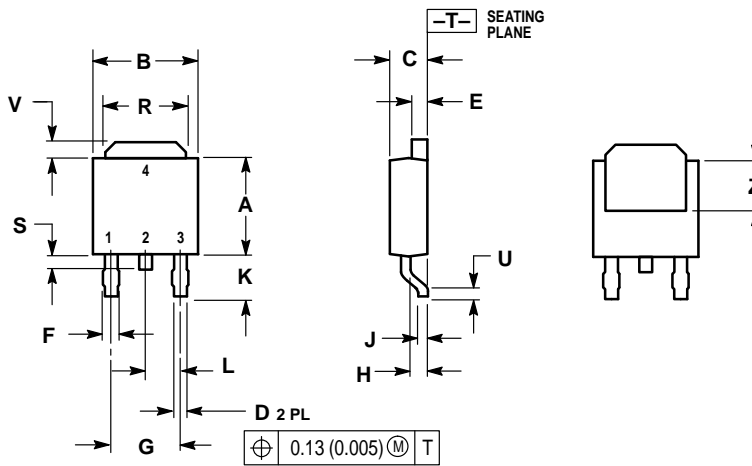


**Figure 10. Active Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS

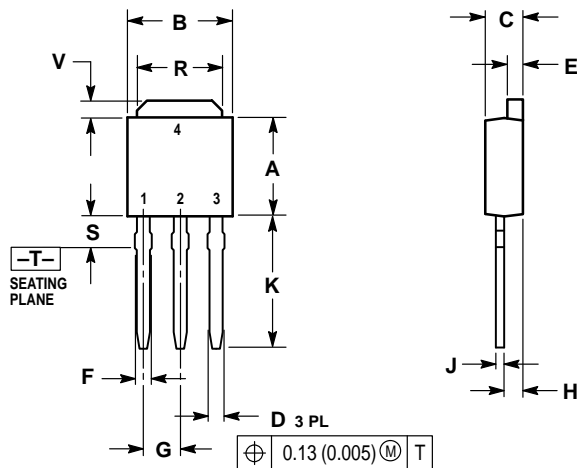


- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020		0.51	
V	0.030	0.050	0.77	1.27
Z	0.138		3.51	

- STYLE 1:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR

CASE 369A-13  
 ISSUE Z




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G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

- STYLE 1:  
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CASE 369-07  
 ISSUE K

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